Real Instruction Set Format

**PDP-8**

- Simplest instruction design for GP computer
- 12-bit fixed length, 12-bit words
- A single GPR, Acc
- Three formats
- Support 35 instructions
- Indirect, displacement, and indexing addressing

**PDP-10**

- Large-scale time-shared system
- Emphasis on making system easy to program, regardless the hardware expenses
- Other elements of an instruction are independent of the opcode
- Each arithmetic data type should have a complete and identical set of operations
- Direct addressing
- 36-bit fixed length, 36-bit word length. 9 bits for opcode, 18 bit address field
PDP-11

- Variable-length
- 13 formats, encompassing 0-, 1-, and 2-address instruction type
- Usually one word (16-bit) long. For multiple memory address instructions, 32- and 48-bit instructions are used
- 6-bit for register reference. 3-bit identify the register (employ 8 16-bit GPRs), 3-bit for addressing mode.
- Instruction set and addressing capability are complex. Increase hardware cost and programming complexity. But more compact program can be developed.

Numbers below fields indicate bit length
Source and destination each contain a 3-bit addressing mode field and a 3-bit register number
FP indicates one of four floating-point registers
R indicates one of the general-purpose registers
CC is the condition code field