Instruction Formats

✧ Defines the layout of bits in an instruction

✧ Includes opcode, and operand(s) (implicitly or explicitly)

✧ Usually more than one instruction format in an instruction set
Instruction Length

- Affected by and affects:
  - Memory size/organization
  - Bus structure
  - CPU complexity/speed

- Tradeoff between powerful instruction set and saving space

- Length and bus size

- Memory bottleneck
Allocation of Bits

- **Fixed length**: tradeoff between the num. of opcodes and the addressing capability

- **Variable-length**: refinement to the tradeoff
  - Minimum opcode length
  - Additional operands for some opcodes
Factors in determine the use of addressing bits

- Number of addressing modes
- Number of operands
- Register v.s. memory
- Number of register sets
- Address range
- Address granularity
PDP-8

- Simplest instruction design for GP computer
- 12-bit fixed length, 12-bit words
- A signal GPR, Acc
- Three formats
- Support 35 instructions
- Indirect, displacement, and indexing addressing

### Memory reference instructions

<table>
<thead>
<tr>
<th>Opcode</th>
<th>D/I</th>
<th>Z/C</th>
<th>Displacement</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
</tbody>
</table>

### Input/output instructions

<table>
<thead>
<tr>
<th>Device</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>8</td>
</tr>
</tbody>
</table>

### Register reference instructions

<table>
<thead>
<tr>
<th>CLA</th>
<th>CLL</th>
<th>CMA</th>
<th>CML</th>
<th>RAR</th>
<th>RAL</th>
<th>BSW</th>
<th>IAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
</tr>
</tbody>
</table>

### Microinstructions

- **Group 1 microinstructions**
  - 1110
  - CLA, CLL, CMA, CML, RAR, RAL, BSW, IAC

- **Group 2 microinstructions**
  - 11110
  - CLA, SMA, SZA, SNL, RSS, OSR, HLT

- **Group 3 microinstructions**
  - 11110
  - CLA, MQA, MQL

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- **D/I** = Direct/Indirect address
- **Z/C** = Page 0 or Current page
- **CLA** = Clear Accumulator
- **CLL** = Clear Link
- **CMA** = Complement Accumulator
- **CML** = Complement Link
- **RAR** = Rotate Accumulator Right
- **RAL** = Rotate Accumulator Left
- **BSW** = Byte SWap
- **IAC** = Increment ACcumulator
- **SMA** = Skip on Minus Accumulator
- **SZA** = Skip on Zero Accumulator
- **SNL** = Skip on Nonzero Link
- **RSS** = Reverse Skip Sense
- **OSR** = Or with Switch Register
- **HLT** = HalT
- **MQA** = Multiplier Quotient into Accumulator
- **MQL** = Multiplier Quotient Load
PDP-10

- Large-scale time-shared system
- Emphasis on making system easy to program, regardless the hardware expenses
- Other elements of an instruction are independent of the opcode
- Each arithmetic data type should have a complete and identical set of operations
- Direct addressing

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Register</th>
<th>I</th>
<th>Index register</th>
<th>Memory address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>8</td>
<td>9</td>
<td>12</td>
<td>14 17 18 35</td>
</tr>
</tbody>
</table>

I = indirect bit

- 36-bit fixed length, 36-bit word length. 9 bits for opcode, 18 bit address field
Variable-length

13 formats, encompassing 0-, 1-, and 2-address instruction type

Usually one word (16-bit) long. For multiple memory address instruction, 32- and 48-bit instructions are used

6-bit for register reference. 3-bit identify the register (employ 8 16-bit GPRs), 3-bit for addressing mode.

Instruction set and addressing capability are complex. Increase hardware cost and programming complexity. But more compact program can be developed.