Sequential Circuits

What is a Sequential Circuits

- Combinational circuits are often referred to as “memoryless” circuits, since their output depends only on their current input and no history of prior inputs is related.
- The current output of a sequential circuit depends not only on the current input, but also on the current state of the circuit.
- The simplest form of sequential circuit is flip-flop.

S-R Latch (S-R flip-flop)

- A most simple type of flip-flop.
- A S-R latch looks like below.

- It has two inputs: S (set), R (reset), and two outputs: Q and Q’.
- The truth table for S-R latch is

<table>
<thead>
<tr>
<th>$S$</th>
<th>$R$</th>
<th>$Q_n$ (current state)</th>
<th>$Q_{n+1}$ (next state)</th>
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<tbody>
<tr>
<td>0</td>
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</table>
- From the table, we can observe that when \( R = 1 \) (reset), \( Q \)'s value will become 0 no matter what is the current value of \( Q \).
- When \( S = 1 \) (set), \( Q \)'s value will become 1 regardless the current value of \( Q \).
- When \( S = R = 0 \), \( Q \)'s value remains the same.
- When \( S = R = 1 \), the outputs of the S-R latch is meaningless, as both \( Q \) and \( Q' \) become 0.

- Therefore, as long as \( S \) and \( R \) stay 0, the S-R latch is bistable.
- This bistable feature enables S-R latch being used as a 1-bit memory.

**Clocked S-R Latch**

- It is often convenient to prevent the latch from changing state except at certain specified times.
- Therefore, the clocked S-R latch is introduced.
- A clocked S-R latch can only be set or reset when the clock is high.
- When the clock is low, \( Q \)'s value remains the same, which is the same as when \( S = R = 0 \).
- A clock is a pulse sequence.

**Locked D Latch**

- There is still a problem with the clocked S-R latch needed to be address, which is that the condition \( S = R = 1 \) must be avoid.
- One way to do this is to allow just a signal input.
Edge-triggered D Latch

- We don’t want to latch onto a value the whole time the clock is high, since the value of D may change during the period.

- We just want to latch onto D on the rising edge of the clock. So we need a pulse generator.

- Take advantage of the propagation delay, we can change the value of D.

- Both b and c have propagation delay. But c’s delay is much shorter than b’s. So we can get a short pulse, and change the value of D during the short period of time.

- We then can connect the input a of the pulse generator to generate a short pulse and use that pulse to control the locked D-latch, shown as below. We call this locked D-latch, edge-triggered D latch or D flip-flop.

- D flip-flop is widely used in computer registers used to temporarily store data.