ISA - Instruction Set Architecture (V)

Addressing Modes (cont.)

Displacement

- **Combines** the capabilities of direct addressing and register indirect addressing.
- Instructions have two address fields, at least one of which (A) is explicit. The other address field (R) can be an implicit reference based on opcode, or can explicitly refer to a register whose contents are added to A to produce the actual address.
- **Advantage:** flexibility
- **Disadvantage:** complexity

**Relative addressing**
- The R field refers to the PC, which is implicitly in the instruction.
- Typically the explicit address field is treated as 2’s complement
- The actual address the operation needs is a displacement relative to the PC’s value that is considered current execution point in a program.
- The actual address is PC’s value + explicit address field value.
- Generally used by control flow instructions

**Indexed addressing**
- The A field refers a main memory address, and the register referred by the R field, usually is the index register, contains a positive displacement from that address
- The actual address is the address in A field + the value in the index register
- Used to access an array whose elements are in successive memory locations. By incrementing or decrementing index register value, different element of the array can be accessed.
- Index register is a general register. It is initialized to 0. After each operation, the index register is incremented by 1.

- **Register base-indexed addressing**
  - Two address fields, A and R, both refer to the registers, which usually are the index register and the base register.
  - Base register: the only general-purpose register (GPR) which may be used for indirect addressing.
  - The actual address is the value in the base register + the value in the index register

- **Register base-scaled indexed addressing**
  - Three address fields, two refer to the registers, one is the scale
  - The actual address is the value in the base register + (the value in the index register x scale)

- Example:
  - Given the following memory values and register values, assume the LOAD instruction loads the value at a specific address to the accumulator based on the addressing mode. What values do the following instructions load into the accumulator?

<table>
<thead>
<tr>
<th>GPRs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
</tr>
<tr>
<td>A</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>D</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Main Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
</tr>
<tr>
<td>100</td>
</tr>
<tr>
<td>101</td>
</tr>
<tr>
<td>110</td>
</tr>
<tr>
<td>111</td>
</tr>
</tbody>
</table>
LOAD Immediate 100       [100]
LOAD Direct 100           [101]
LOAD Indirect 100         [102]
LOAD RegisterDirect C     [110]
LOAD RegisterIndirect C   [103]
LOAD Register Base–Indexed A, D [104]
LOAD Register Base–Scaled Indexed A, B, 2 [103]

Real Instruction Format

PDP-8
- Released in 1965, discontinued in 1970
- Simplest instruction design for general purpose computers
- 12-bit fixed length, 12-bit words
- A single GPR, Accumulator
- Three instruction formats
- Support 35 instructions
- Adopt indirect, displacement, and indexed addressing
**PDP-10**
- Released in 1966, discontinued in 1983
- Designed for large-scale time-shared system
- Emphasis on making system easy to program regardless the hardware expenses
- Other elements of an instruction are independent of the opcode
- Each arithmetic data type should have a complete and identical set of operations
- Direct addressing
- 36-bit fixed length instruction
- 36-bit word length: 9 bits for opcode, 18-bit address field

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Register</th>
<th>I</th>
<th>Index register</th>
<th>Memory address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>8</td>
<td>9</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>14</td>
<td>17</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>35</td>
</tr>
</tbody>
</table>

$I = \text{indirect bit}$

**PDP-11**

Numbers below fields indicate bit length
Source and destination each contain a 3-bit addressing mode field and a 3-bit register number
FP indicates one of four floating-point registers
R indicates one of the general-purpose registers
CC is the condition code field
- Released in 1970, discontinued in early 1990s
- Most popular minicomputer, the first officially named version of Unix ran on it
- Uses variable-length instructions
- 13 instruction formats, encompassing 0-, 1-, and 2-memory address instruction types
- Usually one word (16-bit) long. For multiple memory address instructions, 32- and 48-bit instructions are used
- 6 bits for register reference: 3 bits identify the register (employ 8 16-bit GPRs), and 3 bits for addressing mode
- Instruction set and addressing capability are complex. Increase hardware cost and programming complexity. But more compact program can be developed.