Circuits (I)

Gates

- The logical operations, AND, OR, NOT, are implemented as gates on hardware.
- Gates are fundamental building block of all digital logic circuits.
- Functions (like addition) are implemented by the interconnection of gates.
- A gate is an electronic circuit that produces an output signal that is a simple boolean operation on its input signals.
- A low signal (between 0 and 0.5 voltages) represents 0 (FALSE) and a high signal (between 1 and 1.5 voltages) represents 1 (TRUE).

- Six basic gates used in digital logic.

<table>
<thead>
<tr>
<th>Name</th>
<th>Graphical Symbol</th>
<th>Algebraic Function</th>
<th>Truth Table</th>
</tr>
</thead>
</table>
| AND   | ![AND Gate](image) | \( F = A \cdot B \) or \( F = AB \) | \[
|       |                  |                    | \[
|       |                  |                    | \[
|       |                  |                    | \[
| OR    | ![OR Gate](image) | \( F = A + B \)   | \[
|       |                  |                    | \[
|       |                  |                    | \[
| NOT   | ![NOT Gate](image) | \( F = \overline{A} \) or \( F = A' \) | \[
|       |                  |                    | \[
|       |                  |                    | \[
| NAND  | ![NAND Gate](image) | \( F = \overline{AB} \) | \[
|       |                  |                    | \[
|       |                  |                    | \[
| NOR   | ![NOR Gate](image) | \( F = A + B \)   | \[
|       |                  |                    | \[
|       |                  |                    | \[
| XOR   | ![XOR Gate](image) | \( F = A \oplus B \) | \[
|       |                  |                    | \[
|       |                  |                    | \[

1
Combinational Circuits

Get a Combinational Circuits from a Truth Table

- Taking a look at the basic gate XOR, it actually can be represented by AND and OR gates.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>XOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- Do you see the pattern here?
  - General rule (apply when draw a circuit from a truth table): one OR gate for final output. The OR gate is fed with AND gates, one for each 1 in the output column of the table.