Sequential Circuits (III)

Clocked S-R Latch
- It is often convenient to prevent the latch from changing state except at certain specified times.
- Therefore, the clocked S-R latch is introduced.
- A clocked S-R latch can only be set or reset when the clock is high.
- When the clock is low, Q's value remains the same, which is the same as when S = R = 0.
- A clock is a pulse sequence.

![Clocked S-R Latch Diagram](image)

Locked D Latch
- There is still a problem with the clocked S-R latch needed to be address, which is that the condition S = R = 1 must be avoid.
- One way to do this is to allow just a signal input.

![Locked D Latch Diagram](image)
Edge-triggered D Latch

- We don't want to latch onto a value the whole time the clock is high, since the value of D may change during the period.
- We just want to latch onto D on the rising edge of the clock. So we need a pulse generator.

- Take advantage of the propagation delay, we can change the value of D.

- Both b and c have propagation delay. But c’s delay is much shorter than b’s. So we can get a short pulse, and change the value of D during the short period of time.

- We then can connect the input a of the pulse generator to generate a short pulse and use that pulse to control the locked D-latch, shown as below. We call this locked D-latch, edge-triggered D latch or D flip-flop.

- D flip-flop is widely used in computer registers used to temporarily store data.
Registers

- We know that an edge-triggered D latch (D flip-flop) is a 1-bit memory and can be used to build registers.
- We use a black box representation for this D flip-flop.

![D flip-flop diagram]

- Let's see how to build a 4-bit parallel register using the D flip-flop.

![4-bit parallel register diagram]

- A parallel register consists of a set of D flip-flops that can be read or write simultaneously.
- The clock signal can also be an input of an AND gate coupled with an enable bit. The enable bit is to control writing into the register from D1 to D4, which might be the outputs of an ALU or the outputs of multiplexers, so that data from variety of sources can be loaded into the register.