ISA - Instruction Set Architecture (IV)

Addressing Modes (cont.)

**Register Direct**

- Similar to direct addressing. The only difference is that the address field refers to a register that contains the operand.
- To clarify, if the content of R is 5, then register R5 is the intended address, and the operand value is contained in R5.
- Typically, R is 3 to 5 bits, so that a total of form 8 to 32 general-purpose registers can be referenced.

**Advantages** compared with Direct:
- *small address field in the instruction*
- *no memory reference* (memory reference are time-consuming)

**Disadvantages** compared with Direct: *limited storage space* (limited number of registers compared with main memory locations)

**Register Indirect**

- Diagram showing the register indirect addressing mode.
• Analogous to indirect addressing. The only difference is that the **address field refers to a register**. The value stored in the register is the actual address of the operand in main memory.

• **Advantage compared with Indirect:**
  - *one less memory reference, and smaller address field*

• **Disadvantage compared with Indirect:**
  - limited storage space

**Displacement**

![Displacement Diagram](image)

• **Combines** the capabilities of **direct addressing** and **register indirect addressing**.

• Instructions have **two address fields**, at least one of which (A) is explicit. The other address field (R) can be an implicit reference based on opcode, or can explicitly refer to a register whose contents are added to A to produce the actual address.

• **Advantage:** *flexibility*

• **Disadvantage:** *complexity*

**Relative addressing**

- The R field refers to the PC, which is implicitly in the instruction.
- Typically the explicit address field is treated as 2’s complement
- The actual address the operation needs is a displacement relative to the PC’s value that is considered current execution point in a program.
- The actual address is PC’s value + explicit address field value.
- Generally used by control flow instructions
• Indexed addressing
  - The A field refers a main memory address, and the register referred by the R field, usually is the index register, contains a positive displacement from that address
  - The actual address is the address in A field + the value in the index register
  - Used to access an array whose elements are in successive memory locations. By incrementing or decrementing index register value, different element of the array can be accessed.
  - Index register is a general register. It is initialized to 0. After each operation, the index register is incremented by 1.

• Register base-indexed addressing
  - Two address fields, A and R, both refer to the registers, which usually are the index register and the base register.
  - Base register: the only general-purpose register (GPR) which may be used for indirect addressing.
  - The actual address is the value in the base register + the value in the index register

• Register base-scaled indexed addressing
  - Three address fields, two refer to the registers, one is the scale
  - The actual address is the value in the base register + (the value in the index register x scale)

- Example:
  • Given the following memory values and register values, assume the LOAD instruction loads the value at a specific address to the accumulator based on the addressing mode. What values do the following instructions load into the accumulator?

<table>
<thead>
<tr>
<th>GPRs</th>
</tr>
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<tbody>
<tr>
<td>Address</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>A</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>D</td>
</tr>
</tbody>
</table>
Main Memory

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>101</td>
</tr>
<tr>
<td>101</td>
<td>102</td>
</tr>
<tr>
<td>110</td>
<td>103</td>
</tr>
<tr>
<td>111</td>
<td>104</td>
</tr>
</tbody>
</table>

LOAD Immediate 100 [100]  
LOAD Direct 100 [101]  
LOAD Indirect 100 [102]  
LOAD RegisterDirect C [110]  
LOAD RegisterIndirect C [103]  
LOAD Register Base–Indexed A, D [104]  # A is base reg. and D is index reg.  
LOAD Register Base–Scaled Indexed A, B, 2 [103]  # A is base reg. and B is index reg.