

VHDL (II)

A Full Adder (cont.)

- The adder we discussed is a half adder. Why “half”? [A full adder would have a carry in as well]
 - A full adder can be implemented as two half-adders and one OR gate.
 - The SUM output of the full add is XOR on the SUM output of the half add and the carry in.
 - The Carry out is 1 if either A and B are both 1 (left input to the OR gate) or exactly one of them is 1 and the Carry In bit is also 1.

A	B	Carry in	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

