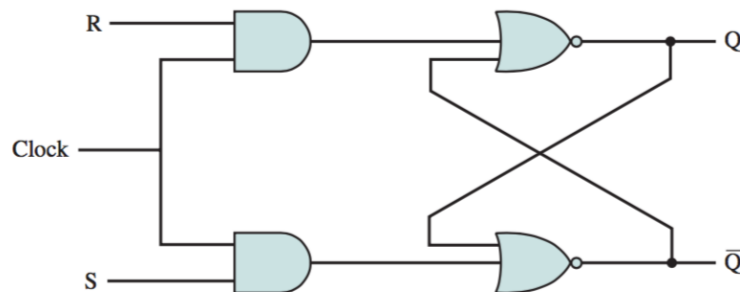


Sequential Circuits (III)

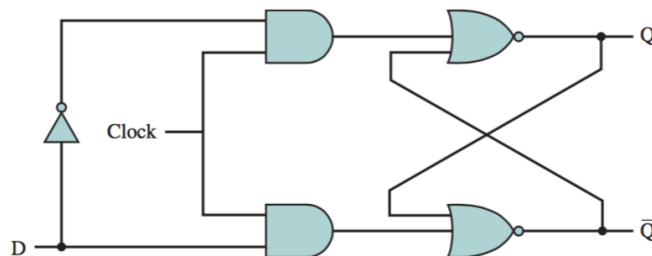
Clocked S-R Latch

- It is often convenient to prevent the latch from changing state except at certain specified times.
- Therefore, the clocked S-R latch is introduced.
- A clock is a sequence that changes from 1 to 0 at a regular interval. 
- A clocked S-R latch can only be set or reset when the clock is high.
- When the clock is low, Q's value remains the same, which is the same as when $S = R = 0$. So, we can reach a bistable state when clock is 0.
- Also, when clock is 0, the meaningless state won't be triggered as well. However, we also want the meaningless state cannot be triggered when clock is high. How can we modify the clocked S-R latch to achieve it. Hint: we don't want S and R both equal to 1 at the same time. Observe S and R's values for Set and Reset. You will find the R is the negation of S.



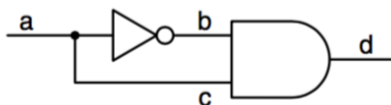
Locked D Latch

- One way to avoid the meaningless state is to allow just a signal input.

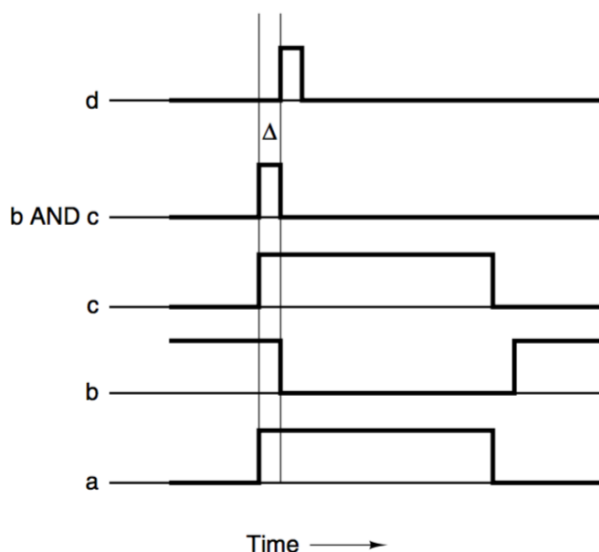


Edge-triggered D Latch

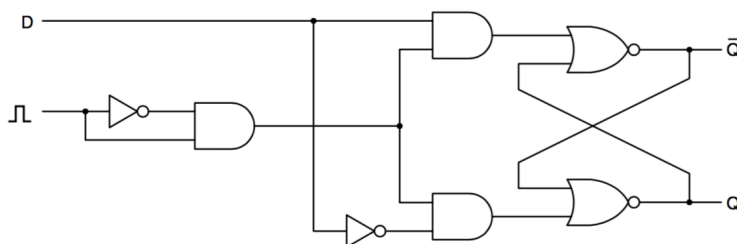
- We don't want to latch onto a value the whole time the clock is high, since the value of D may change during the period.
- We just want to latch onto D on the rising edge of the clock. So we need a pulse generator.



- Take advantage of the propagation delay, we can change the value of D during the rising edge of the clock.



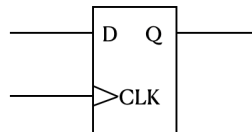
- Both b and c have propagation delay. But c's delay is much shorter than b's. So we can get a short pulse, and change the value of D during the short period of time.
- We then can connect the clock to the input a of the pulse generator to generate a short pulse and use that pulse to control the locked D-latch, shown as below. We call this locked D-latch, **edge-triggered D latch** or **D flip-flop**.



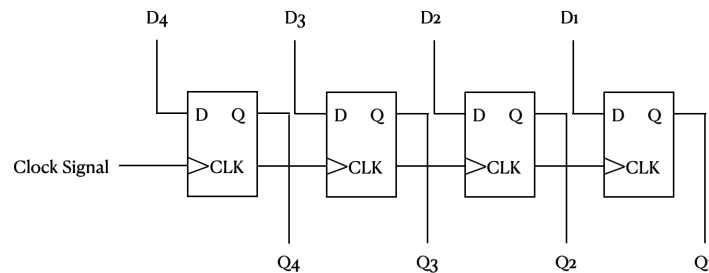
- D flip-flop is widely used in computer registers used to temporarily store data.

Registers

- We know that an edge-triggered D latch (D flip-flop) is a 1-bit memory and can be used to build registers.
- We use a black box representation for this D flip-flop.



- Let's see how to build a 4-bit parallel register using the D flip-flop.



- A **parallel register** consists of a set of D flip-flops that can be read or write simultaneously.
- The clock signal can also be an input of an AND gate coupled with an **enable bit**. The enable bit is to **control writing** into the register from D1 to D4, which might be the outputs of an ALU or the outputs of multiplexers, so that data from variety of sources can be loaded into the register.