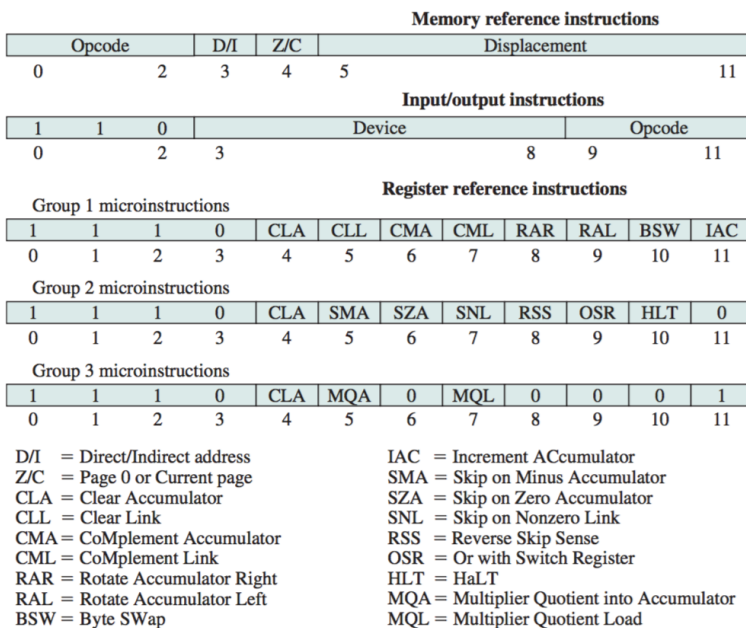


ISA - Instruction Set Architecture (VI)

Real Instruction Formats

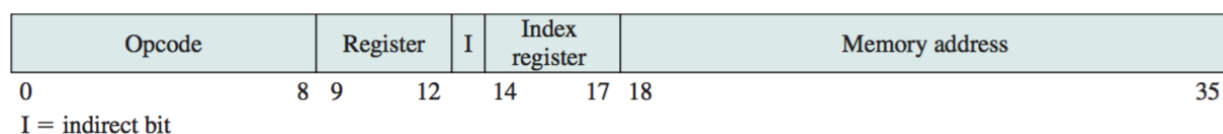
PDP-8

- Released in 1965, discontinued in 1970
- Simplest instruction design for general purpose computers
- 12-bit fixed length, 12-bit words
- A single GPR, Accumulator
- Three instruction formats



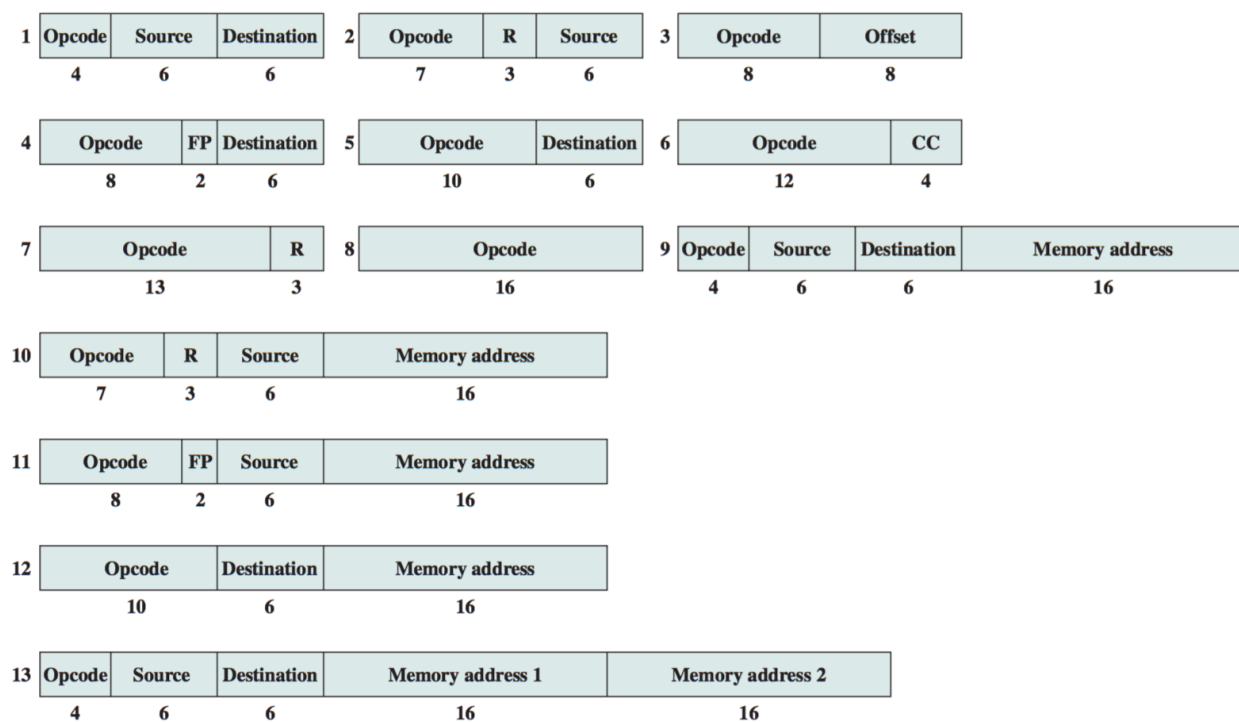
PDP-10

- Released in 1966, discontinued in 1983
- Designed for large-scale time-shared system
- Emphasis on making system easy to program regardless the hardware expenses
- Other elements of an instruction are independent of the opcode
- Each arithmetic data type should have a complete and identical set of operations
- 36-bit fixed length instruction
- 36-bit word length: 9 bits for opcode, 18-bit address field



PDP-11

- Released in 1970, discontinued in early 1990s
- Most popular minicomputer, the first officially named version of Unix ran on it
- Uses variable-length instructions
- 13 instruction formats, encompassing 0-, 1-, and 2-memory address instruction types
- Usually one word (16-bit) long. For multiple memory address instructions, 32- and 48-bit instructions are used
- 6 bits for register reference: 3 bits identify the register (employ 8 16-bit GPRs), and 3 bits for addressing mode
- Instruction set and addressing capability are complex. Increase hardware cost and programming complexity. But more compact program can be developed.



Numbers below fields indicate bit length

Source and destination each contain a 3-bit addressing mode field and a 3-bit register number

FP indicates one of four floating-point registers

R indicates one of the general-purpose registers

CC is the condition code field